APPENDIX C

Reverse Recovery Time (T_{RR})

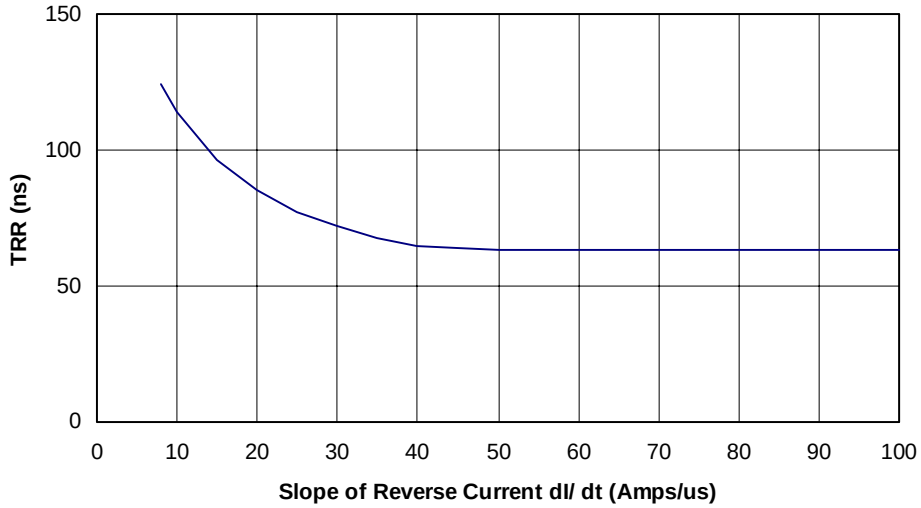
Factors Influencing Reverse Recovery Time

Circuit/Environmental Influences:
a) dl/dT
b) Junction Temperature

Other Factors:
c) Silicon Resistivity
d) Peak Inverse Voltage
e) Manufacturing Process

Circuit Effects: dl/dT

In general, T_{RR} decreases as dl/dT increases. The rate of change varies with the manufacturing process and the speed of the device. Typically, slower devices exhibit less change in T_{RR} as dl/dT changes. The following example reflects data taken from a high-speed, 1000V, 3Amp, platinum-doped, VMI power rectifier:



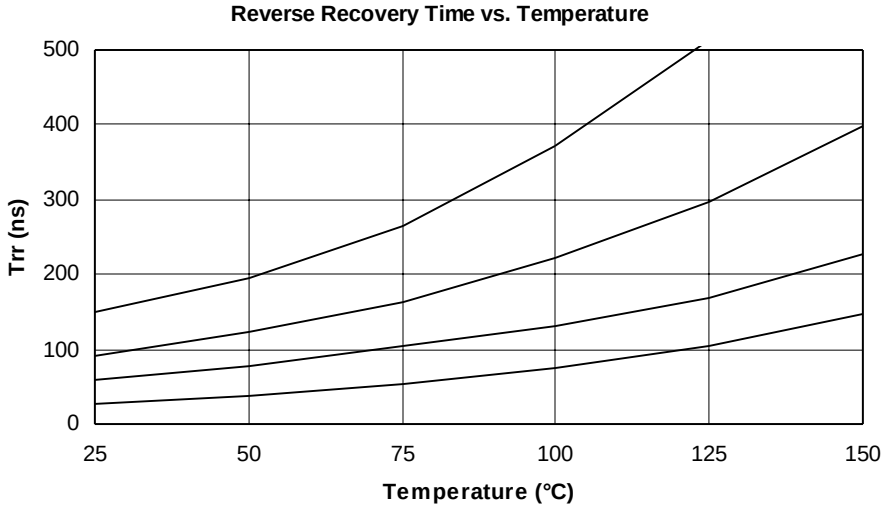
Environmental Effects: Junction Temperature

Typically, T_{RR} increases with junction temperature. The rate of change varies with the manufacturing process and the speed of the device. Higher speed devices, of the same manufacturing process, change more with temperature than slower devices.

Appendix C: Reverse Recovery Time

Environmental Effects: Junction Temperature (continued)

The following graph reflects data taken from a range of VMI fast and ultra-fast diodes.



Other Factors: Silicon Resistivity

In general, T_{RR} increases as silicon resistivity increases. The primary factor is the level of doping during the silicon ingot growing process. (Subsequent doping at the wafer level may yield greater variations in T_{RR} than during ingot manufacturing.)

Other Factors: Peak Inverse Voltage (PIV)

As PIV increases, T_{RR} generally increases. The primary factor is the high resistivity of the starting material. Fewer recombination centers available to sweep out the junction area also contributes to slower devices.

Appendix C: Reverse Recovery Time

Other Factors: Manufacturing Process

Many processes are used to manufacture high speed devices (e.g. platinum doping, gold doping, irradiation, etc.). Each process results in different diode behavior. VMI uses a platinum diffusion technique to optimize the following characteristics:

a) **Low Reverse Leakage** - typically < 1µA at the rated voltage and at room temperature. (Other processes may exhibit > 1mA at the rated voltage and at room temperature.)

b) **Low High Temp Reverse Leakage** - typically < 20µA at the rated voltage and at a junction temperature of 100°C. Thermal runaway, due to reverse leakage, is rarely seen on VMI devices operated within the rated parameters and at temperatures of up to +175°C.

c) **High Voltage** - the VMI platinum doping process provides high voltage break down characteristics exceeded by no other manufacturer of simliar devices.

APPENDIX D

Screening Guides

The following screening procedures are suggested guides for assemblies and their components:

HRP 101: Screening Guide for Discrete Diodes
HRP 102: Screening Guide for Finished Bridge Rectifier Assemblies
HRP 103: Screening Guide for Capacitors Used in Multiplier Assemblies
HRP 104: Screening Guide for Resistors Used in Multiplier Assemblies
HRP 105: Screening Guide for Multiplier Assemblies

HRP 101: Discrete Diodes

The following screening for discrete diodes is a guide for a suggested procedure. It can be modified or adjusted to suit requirements. This is taken from MIL-PRF-19500 Table IV, JANTX screening.

1)	High Temperature Life (non-operating life/ stabilization bake MIL-STD-750)	Method 1032	48 hrs @ +175°C
2)	Temperature Cycling MIL-STD-750	Method 1051 Condition C	20 Cycles -65°C to +175°C 15 min. extremes No dwell @25°C
3)	Interim Electrical		Forward Voltage Drop Leakage Current
4)	High Temperature Reverse Bias (HTRB) MIL-STD-750	Method 1038 Condition A	96 hrs min. @ TA=150°C and min. applied voltage at 80% of rated VR (TC or TL is optional)
5)	Final Electrical MIL-STD-750	Method 4011 Method 4016 Method 4031 Method 4021	Forward Voltage Drop Leakage Current Reverse Recovery Time Peak Inverse Voltage

Appendix D: Screening Guides

HRP 102: Finished Bridge Rectifier Assemblies

The following screening for bridge assemblies is a guide for a suggested procedure. It can be modified or adjusted to suit requirements. This is taken from MIL-PRF-19500 Table IV, JANTX screening.

1)	High Temperature Life (non-operating life/ stabilization bake MIL-STD-750)	Method 1032	24 hrs @ 125°C
2)	Temperature Cycling MIL-STD-202	Method 107 Condition C	10 Cycles -55°C to +125°C 15 min. extremes
3)	Interim Electrical		Forward Voltage Drop Leakage Current
4)	High Temperature Reverse Bias (HTRB) MIL-STD-750	Method 1038 Condition A	24 hrs @ +125°C at 80% of VRWM
5)	Final Electrical MIL-STD-750	Method 4011 Method 4016 Method 4021	Forward Voltage Drop Leakage Current Breakdown Voltage
6)	Visual Mechanical Inspection	Per Specification	Per Specification

Appendix D: Screening Guides

HRP 103: Capacitors Used in Multiplier Assemblies

The following screening for capacitors is a guide for a suggested procedure. It can be modified or adjusted to suit requirements. Capacitors would be screened prior to assembly into a hi-rel multiplier application.

1)	Visual Inspection		Per Specification
2)	High Temp Storage MIL-STD-750	Method 1032	48 hours @ TA = 150°C
3)	Pre Electrical		Capacitance Dissipation
4)	Corona Test		≤ 100 Picocoulombs at rated voltage
5)	Temp Cycle MIL-STD-202	Method 107	5 Cycles, -55°C to +150°C 15 minutes at each extreme No dwell @ 25°C
6)	Post Electrical		Capacitance Dissipation

HRP 104: Resistors Used in Multiplier Assemblies

The following screening for resistors is a guide for a suggested procedure. It can be modified or adjusted to suit requirements. Resistors would be screened prior to assembly into a hi-rel multiplier application.

1)	Pre Electrical		Voltage = rated @25°C Measurement current, resistance
2)	Temperature Cycle MIL-STD-202	Method 107	5 Cycles, -55°C to +150°C 15 minutes at each extreme No dwell @ 25°C
3)	Post Electrical		Voltage = rated @25°C Measurement current, resistance
4)	Visual Inspection		Surface under microscope for cracks, chips, etc.

Appendix D: Screening Guides

HRP 105: Finished Multiplier Assemblies

The following screening for multiplier assemblies is a guide for a suggested procedure. It can be modified or adjusted to suit requirements for a hi-rel multiplier application.

1)	Pre-pot Visual MIL-STD-750	Method 2071	
2)	High Temp Life MIL-STD-750	Method 1032	48 hours @ TA =125°C
3)	Temperature Cycling MIL-STD-750	Method 107	10 Cycles -55°C to +105°C 15 minutes at extremes
4)	Pre-Electrical		Voltage - in per spec Voltage - out per spec Current - out per spec Voltage ripple per spec
5)	Burn-in		48 hours @ TA =85°C Voltage - out Current - out
6)	Post Electrical		Voltage - in per spec Voltage - out per spec Current - out per spec Voltage ripple per spec